S-MOS SYSTEMS
A Seiko Epson Affiliate

Data Sheet **Graphics**

SED1742/44

June 1997

CMOS 160-BIT SEGMENT DRIVER HIGH VOLTAGE LCD DRIVER

■ DESCRIPTION

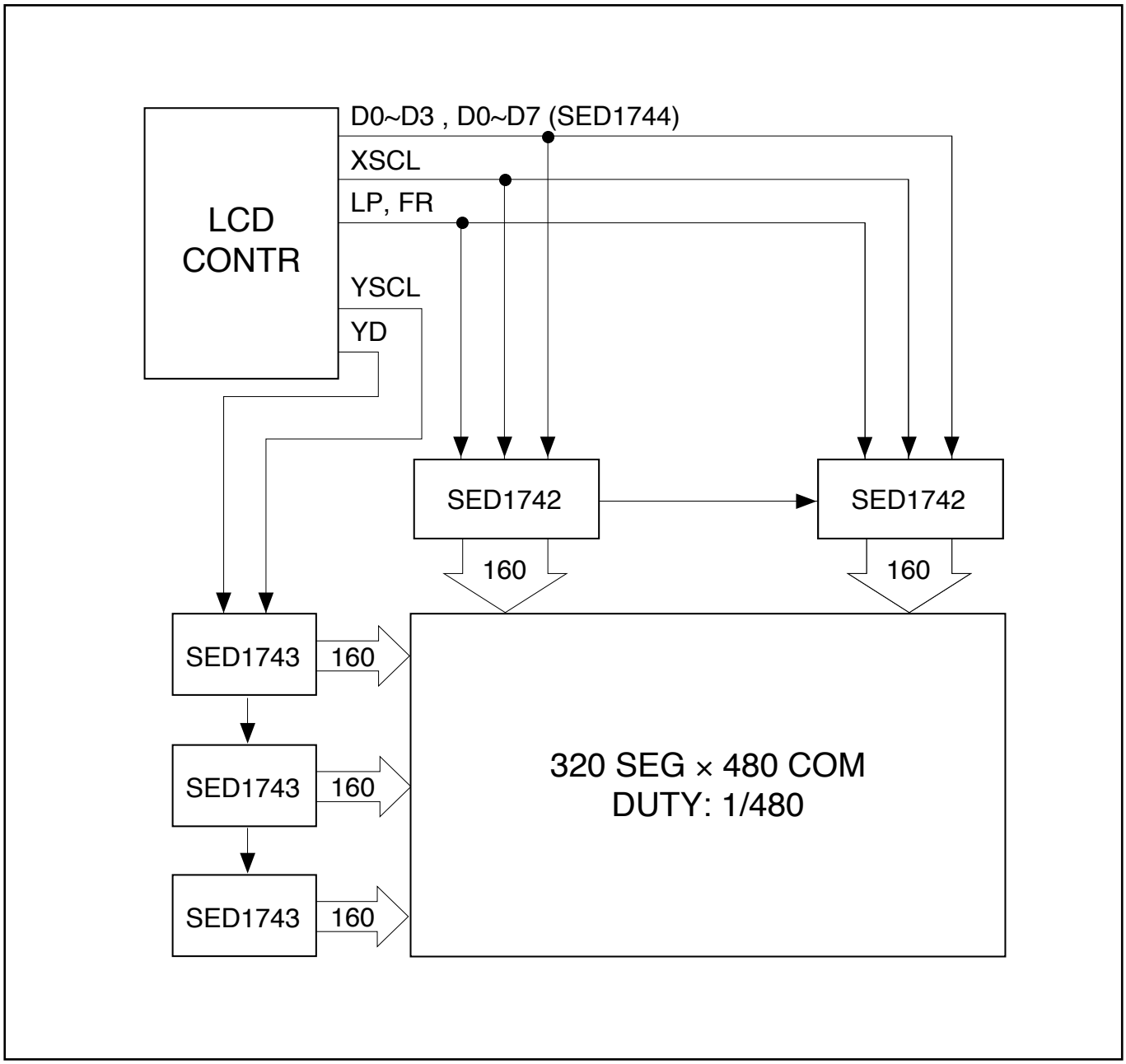
The SED1742/SED1744 is a 160 dot matrix LCD segment (column) driver for driving high-capacity LCD panels at duty cycles higher than 1/100 (up to 1/500). The LSI features a wide range of LCD voltages. The upper and lower LCD drive voltages (V0, V5) are independent of the chip supplies. This enables the LCD drive bias voltages to be supplied from an external source. The device uses a daisy-chain enable system which decreases power consumption and eliminates the need for separate enable signals for each driver.

The SED1742/44 is used in conjunction with the SED1743 (160-bit common driver) to drive a large-capacity dot matrix LCD panel.

■ FEATURES

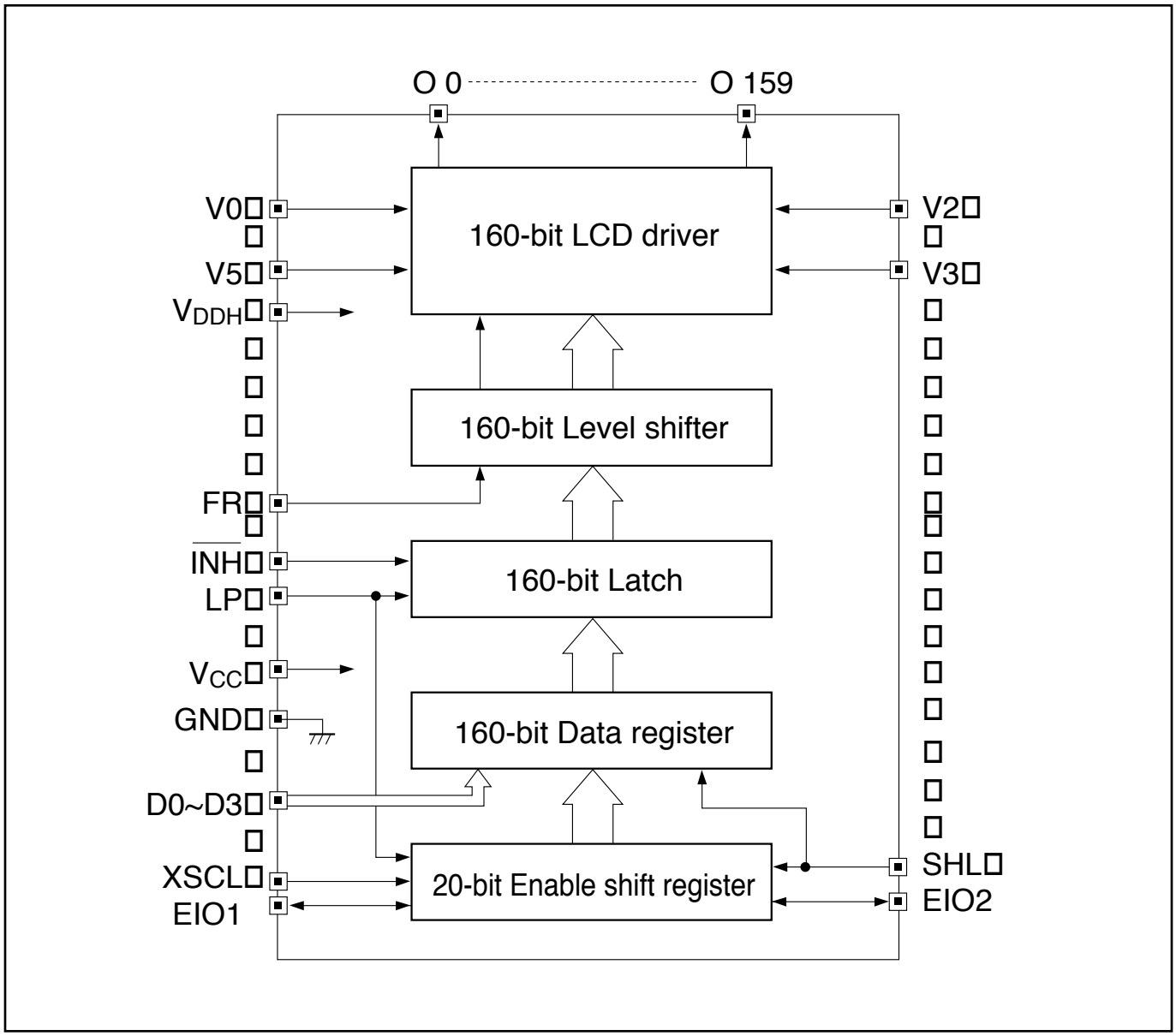
- Low-power high-speed CMOS technology
- 160-bit segment (column) driver
- High-speed data bus 4-bit (SED1742)
  8-bit (SED1744)
- Duty cycle ..... 1/100 to 1/500
- Adjustable LCD drive voltages
- Unbiased display off function
- Adjustable offset bias of the LCD according to V_{DDH} and GND
- Shift clock frequency ..... 12MHz max at V_{DD} = 5V
- Ability to adjust offset bias of the LCD source from V_{DD}
- Daisy chain enable support
- No enable signal by controller is required
- Wide range of LCD voltage ..... 14 to 40V
- Supply voltage ..... 2.7 to 5.5V
- Package ..... TAB (TOA)
  Au bump (D1B)

■ SYSTEM BLOCK DIAGRAM



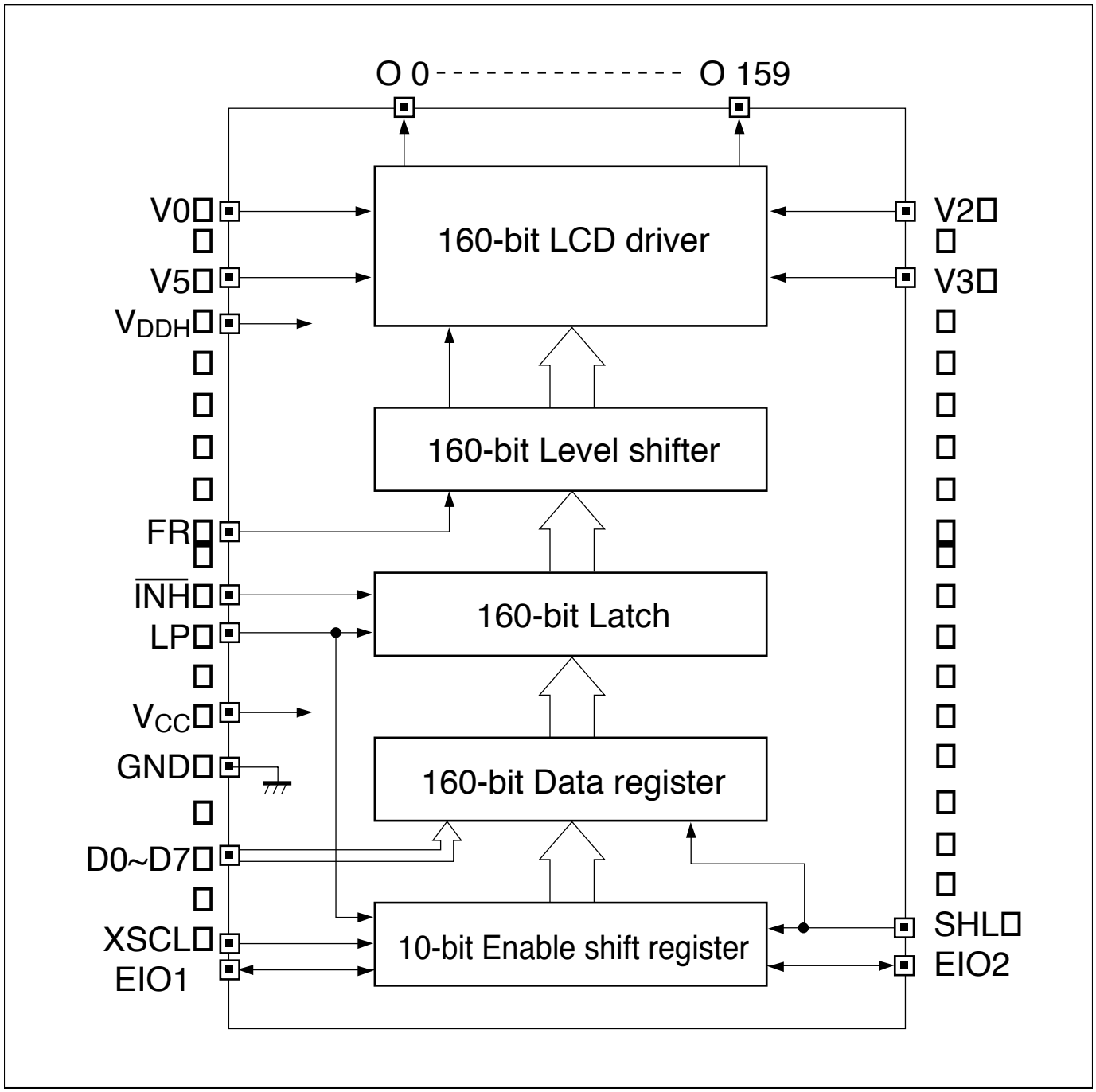
■ BLOCK DIAGRAM

• SED1742



■ BLOCK DIAGRAM

• **SED1744**



■ PIN DESCRIPTION

<table>
<tr><th>Pin Name</th><th>I/O</th><th>Function</th><th>Q'ty</th></tr>
<tr><td>O0 to 159</td><td>—</td><td>LCD crystal segment (column) output
The output varies at the LP trailing edge.</td><td>160</td></tr>
<tr><td>D0 to D3
(SED1742)</td><td>I</td><td>Display data input</td><td>4</td></tr>
<tr><td>D0 TO D7
(SED1744)</td><td>I</td><td>Display data input</td><td>8</td></tr>
<tr><td>XSCL</td><td>I</td><td>Display data shift clock input (triggered at the trailing edge)</td><td>1</td></tr>
<tr><td>LP</td><td>I</td><td>Display data latch pulse input (triggered at the trailing edge)</td><td>1</td></tr>
<tr><td>EI01, EI02</td><td>I/O</td><td>Enable I/O. Set to input or output according to SHL input level. The output is reset at the LP input and set to “L” when a 160-bit data fetch is complete.</td><td>2</td></tr>
<tr><td>SHL</td><td>I</td><td>Shift direction selection and EIO terminal I/O control input (SED1744)
When the data (a, b, .. g, h) (i, .. o, p) ... (s, t, .. y, z) are input in this sequence to the terminals (D0, D1, .. D7), the relation between the data and the segment output is as shown in the table below.

<table>
<tr><th rowspan="2">SHL</th><th colspan="9">O (SEG Output)</th><th colspan="2">EIO</th></tr>
<tr><th>159</th><th>158</th><th>157</th><th>156</th><th>155</th><th>.....</th><th>2</th><th>1</th><th>0</th><th>1</th><th>2</th></tr>
<tr><td>L</td><td>a</td><td>b</td><td>c</td><td>d</td><td>e</td><td>.....</td><td>x</td><td>y</td><td>z</td><td>Output</td><td>Input</td></tr>
<tr><td>H</td><td>z</td><td>y</td><td>x</td><td>w</td><td>v</td><td>.....</td><td>c</td><td>b</td><td>a</td><td>Input</td><td>Output</td></tr>
</table>

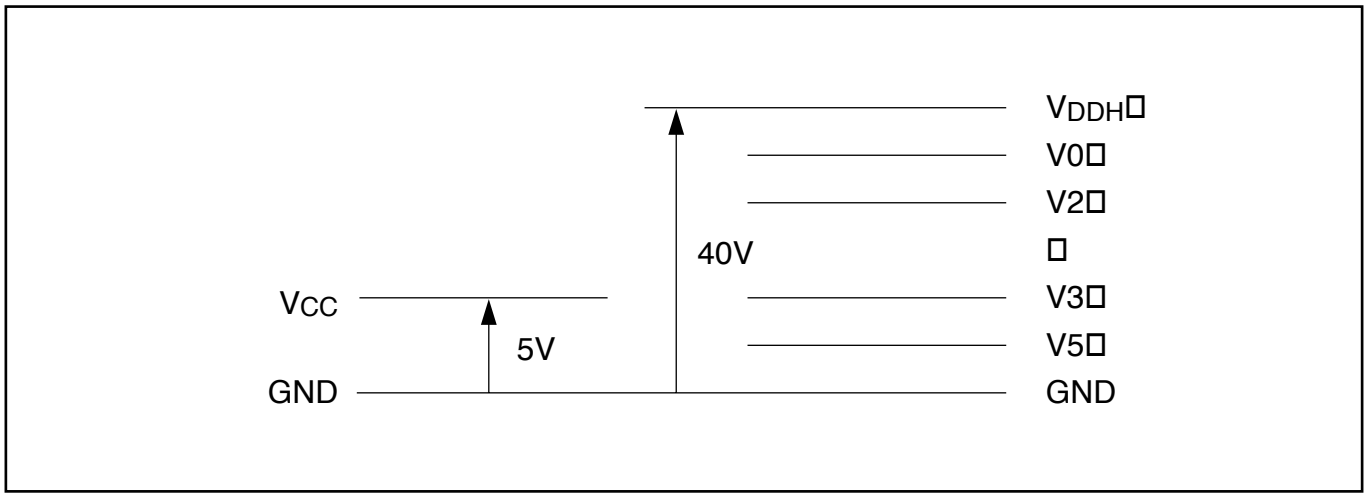
Note: The relation between the data and the segment output is determined independently of the number of shift locks.</td><td>1</td></tr>
<tr><td>FR</td><td>I</td><td>Input of signal to AC electrify the liquid crystal drive output</td><td>1</td></tr>
<tr><td>VCC, GND</td><td>Power Source</td><td>Logic power source. GND: 0 V; VCC: +3, +5 V</td><td>2</td></tr>
<tr><td>V0, V2, V3, V5, V_{DDH}</td><td>Power Source</td><td>Liquid crystal drive power source V_{DDH}: +14 V to 40 V; GND: 0 V
$V_{DDH} \geq V0 > V2 \geq 7/9\ V_{DDH}$, $2/9\ V_{DDH} \geq V3 > V5 \geq GND$</td><td>5</td></tr>
<tr><td>$\overline{INH}$</td><td>I</td><td>Forced blank input
The signal forces the output to be set to V5 level at the “L” level.</td><td>1</td></tr>
<tr><td>TEST</td><td></td><td>Test input normally fixed at “L” level.</td><td>1</td></tr>
</table>

■ ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

Parameter	Symbol		Unit
Supply voltage range (1)	V_{CC}	–0.3 to +7.0	V
Supply voltage for LCD (1)	V_{DDH}	–0.3 to +45.0	V
Supply voltage for LCD (2)	V0, V2, V3, V5	GND –0.3 to V_{DDH} +0.3	V
Input voltage (4)	V_I	GND –0.3 to V_{CC} +0.3	V
Output voltage	V_O	GND –0.3 to V_{CC} +0.3	V
EIO output current	I_{OI}	20	mA
Operating temperature	T_{opr}	–20 to +75	°C
Storage temperature 1 (3)	T_{stg1}	–65 to +150	°C
Storage temperature 2 (3)	T_{stg2}	–55 to +150	°C
Logic supply	V_{CC}	3*	V
Segment driver supply voltage range	V_{DDH}	14 to 28*	V

*Ta = 25°C



Notes: 1. The voltage is based at GND = 0 V

2. Voltage V0, V2, V3 and V5 should satisfy the condition: $V_{DDH} \geq V0 \geq V2 \geq V3 \geq V5 \geq GND$.

3. The storage temperature 1 is specified for a single chip and the storage temperature 2 is for TCP mounting.

4. WARNING: The LSI may be externally broken if the logic system power source floats or decreases below V_{CC} = 2.9 V while voltage is applied to the liquid crystal drive system power source. Special care should be taken for the power source sequence when turning the system power on and off

● DC Electrical Characteristics

Parameter	Symbol	Condition		Terminal	Min	Typ	Max	Unit
Logic supply voltage (1)	V_{CC}			V_{CC}	3.0	5.0	5.5	V
Operation voltage recommended	V_{DDH}			V_{DDH}	14.0	—	40.0	V
Segment driver input supply voltage	V_{DDH}	Function		V_{DDH}	8.0	—	—	V
Segment driver input supply voltage (2)	V0	Value recommended		V0	V_{DDH} –2.5	—	V_{DDH}	V
Segment driver input supply voltage (2)	V2	Value recommended		V2	$7/9V_{DDH}$	—	—	V
Segment driver input supply voltage (2)	V3, V5	Value recommended		V3, V5	GND	—	$2/9V_{DDH}$	V
High-level input voltage	V_{IH}	V_{CC} = 3.0 to 5.5 V		EIO1, EIO2, D0 to D3: SED1742 D0 to D7: SED1744 XSCL, LP, SHL, FR, $\overline{INH}$	$0.8V_{CC}$	—	—	V
Low-level input voltage	V_{IL}				—	—	$0.2V_{CC}$	V
High-level output voltage	V_{OH}	V_{CC} = 3 to 5.5 V	I_{OH} = –0.6 mA	EIO1, EIO2	V_{CC} –0.4	—	—	V
Low-level utput voltage	V_{OL}		I_{OL} = 0.6 mA			—	0.4	V
Low-level input leakage current	I_{LI}	GND ≤ V_{IN} ≤ V_{CC}		D0 to D3: SED1742 D0 to D7: SED1744 LP, FR, XSCL, SHL, $\overline{INH}$	—	—	2.0	µA
Input: leakage current output	$I_{LI/O}$	GND ≤ V_{IN} ≤ V_{CC}		EIO1, EIO2	—	—	5.0	µA
Static current	I_{GND}	V_{DDH} = 14.0 to 40.0 V V_{IH} = V_{CC}, V_{IL} = GND		GND	—	—	25	µA
Output resistance	R_{SEG}	ΔV_{ON}= 0.5V condition recommended	V_{DDH}=+30.0V	O0 to O159	—	0.9	2.5	kΩ
			V_{DDH}=+20.0V		—	1.0	3.0	

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Parameter	Symbol	Condition	Terminal	Min	Typ	Max	Unit
Average Operation current consumed (1)	I_{CC}	V_{CC} = +5.0 V, V_{IH} = V_{CC}, V_{IL} = GND, f_{XSCL} =5.38 MHz, f_{LP} =33.6 kHz, f_{FR} =70 Hz Input data: Display checkered, No load	V_{CC}	—	0.4	1.2	mA
		V_{CC} = +3.0 V; Other condi tions: same as V_{CC} = +5.0 V		—	0.2	0.6	
Average Operation current consumed (2)	I_{DDH}	V_{DDH} = V0 = +30.0 V, V_{CC} = +5.0 V, V3 = +4.0 V, V2 = +26.0 V, V5 = 0.0 V; Other conditions: same as V_{CC} = +5.0 V	V_{DDH}	—	0.5	1.5	mA
Input capacitance	C_I	Freq.=1 MHz, Ta = 25°C Single chip	D0 to D3: SED1742 D0 to D7: SED1744 LP, FR, XSCL, SHL, $\overline{INH}$	—	—	8	pF
I/O terminal capacity	$C_{I/O}$		EIO1, EIO2	—	—	15	pF

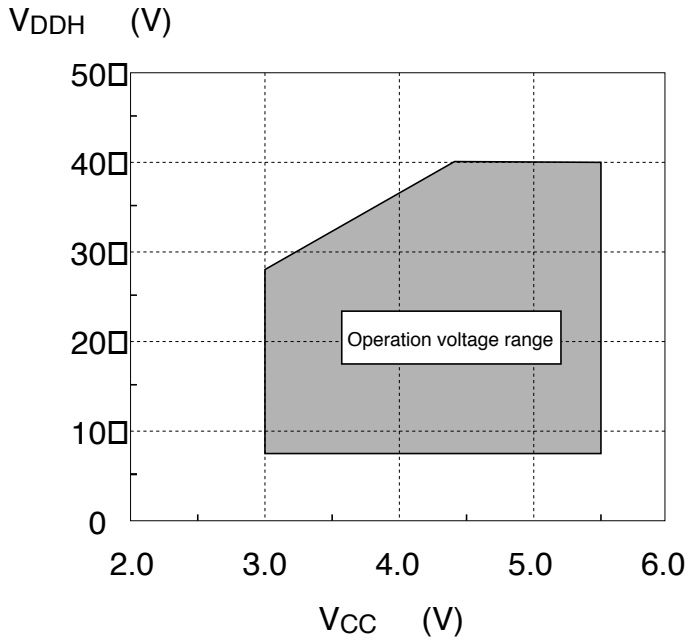
Notes: 1. The voltage is based at GND = 0 V

2. Voltage V0, V2, and V3 should satisfy the condition: VDDH ≥ V0 ≥ V2 ≥ V3 ≥ V5 ≥ GND.

● Operating Voltage Range VCC–VDDH

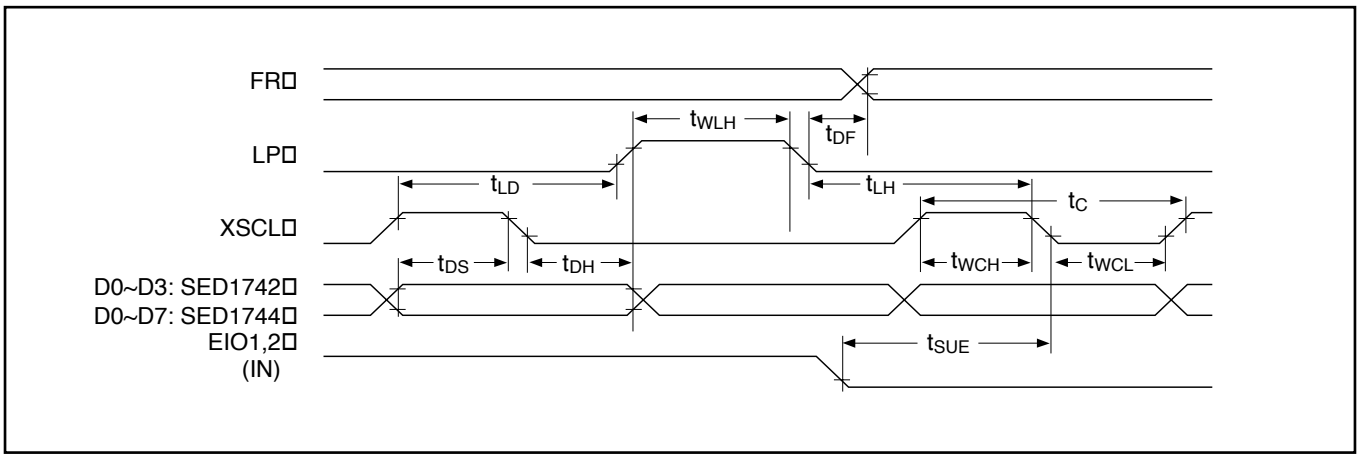
The maximum LCD supply voltage, V_{DDH} depends on V_{CC} as shown in the following figure.

Specify the V_{DDH} voltage within the V_{CC}–V_{DDH} operation.



● AC Electrical Characteristics

Input Timing Characteristics



Note: Adjust the timing of the LP pulse input at high-speed operation, excluding one clock of XSCL.

(V_{CC} = 5.0 V ±10%, Ta = –20 to 75°C)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
XSCL cycle	t_C		83	—	—	ns
XSCL high-level pulse width	t_{WCH}		30	—	—	ns
XSCL low-level pulse width	t_{WCL}		30	—	—	ns
Data setup time	t_{DS}		30	—	—	ns
Data hold time	t_{DH}		30	—	—	ns
XSCL ---> LP rise time	t_{LD}		–5	—	—	ns
LP ---> XSCL breaking time	t_{LH}		60	—	—	ns
LP high-level pulse width (1)	t_{WLH}		45	—	—	ns

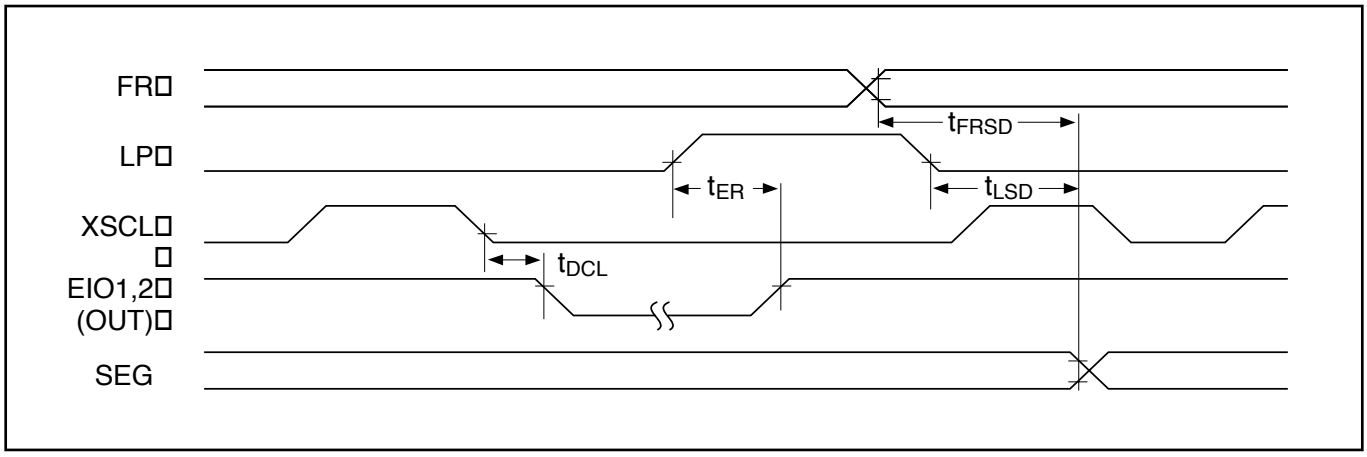
Note: t_{WLH} defines the time duration when the LP is “H” and the XSCL is “L”

(V_{CC} = 3.0 to 4.5 V, Ta = –20 to 75°C)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
XSCL cycle	t_C		125	—	—	ns
XSCL high-level pulse width	t_{WCH}		50	—	—	ns
XSCL low-level pulse width	t_{WCL}		50	—	—	ns
Data setup time	t_{DS}		50	—	—	ns
Data hold time	t_{DH}		30	—	—	ns
XSCL ---> LP rise time	t_{LD}		0	—	—	ns
LP ---> XSCL breaking time	t_{LH}		120	—	—	ns
LP high-level pulse width (1)	t_{WLH}		90	—	—	ns
FR delay allowance time	t_{DF}		–600	—	600	ns
EIO setup time	t_{SUE}		70	—	—	ns

Note: t_{WLH} defines the time duration when the LP is “H” and the XSCL is “L”

° Output Timing Characteristics



(V_{CC} = +5.0 V ±10%, V_{DDH} = 14.0 to 40.0 V)

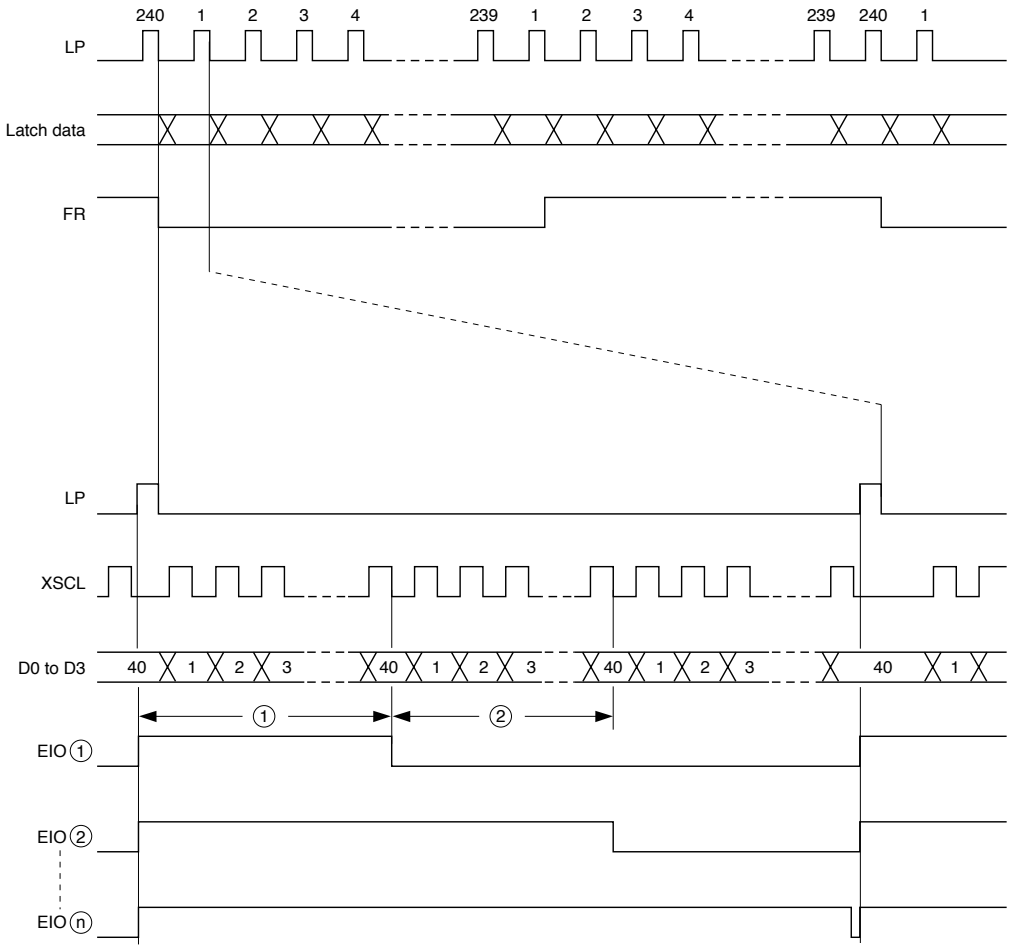
Parameter	Symbol	Condition	Min	Typ	Max	Unit
EIO reset time	t_{ER}	C_L = 15 pF (EIO)	—	—	120	ns
EIO output delay time	t_{DCL}		—	—	45	ns
LP ---> SEG output delay time	t_{LSD}	C_L = 100 pF (On)	—	—	200	ns
FR ---> SEG output delay time	t_{FRSD}		—	—	400	ns

(V_{CC} = +5.0 V ±10%, V_{DDH} = 14.0 to 40.0 V)

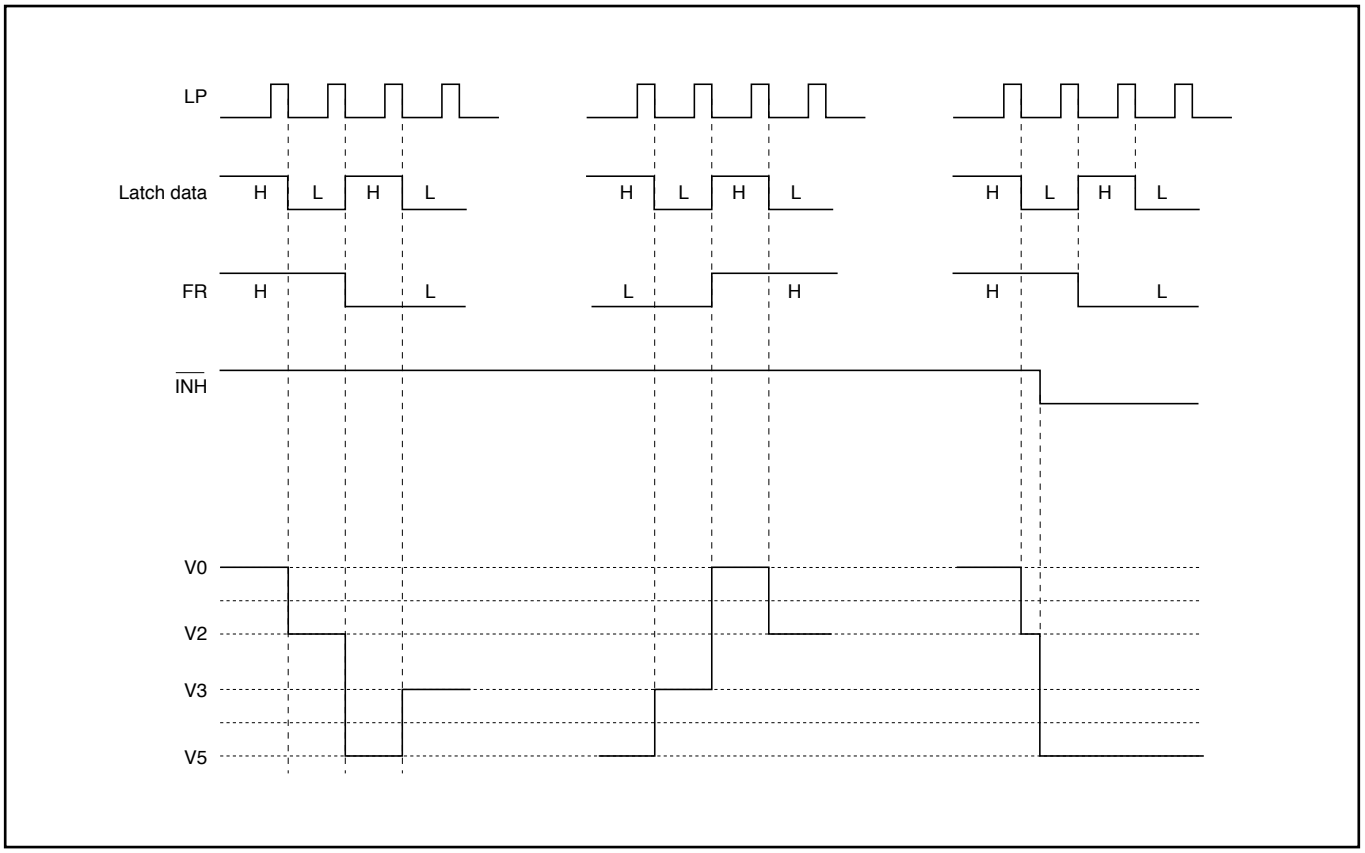
Parameter	Symbol	Condition	Min	Typ	Max	Unit
EIO reset time	t_{ER}	C_L = 15 pF (EIO)	—	—	120	ns
EIO output delay time	t_{DCL}		—	—	45	ns
LP ---> SEG output delay time	t_{LSD}	C_L = 100 pF (On)	—	—	200	ns
FR ---> SEG output delay time	t_{FRSD}		—	—	400	ns

● Timing Diagrams

° 1/240 Duty Cycle



Notes:
1. The circled numerals 1 to n denote the position of the device in the chain.
2. One cycle of XSCL should be lengthened tio satisfy t_{LH} when high-speed data transfer takes place.


LP
Latch data
H
L
H
L
FR
H
L
INH
V0
V2
V3
V5

■ FUNCTIONAL DESCRIPTION

● Enable Shift Register

The enable shift register is a bi-directional shift register, where the shift direction is selected by SHL. SHL is also used to latch data from the data bus into the data register. The effect of SHL on the shift direction and on the input data sequence is shown in the following table.

Data Sequence and Shift Direction

SHL	LCD Outputs							Shift Direction	
	O159	O158	O157	...	O2	O1	O0	EIO1	EIO2
L	a	b	c	...	x	y	z	Output	Input
H	z	y	x	...	c	b	a	Input	Output

When the enable signal is inactive, the SED1742 is in standby mode with the internal clock stopped and the data bus held LOW. When multiple SED1742s are used, the enable input of the first device should be connected to ground and the enable input of each successive device should be connected to the enable output of the preceding device.

When 160 data bits have been latched into the SED1742, the enable output edge goes LOW, eliminating the need for an external control circuit.

● Data Register

The data register converts the input data into parallel display driver data under the control of the enable shift register.

■ APPLICATION NOTES

● Voltage Levels

The recommended method of generating the LCD drive voltages, V0 to V5, is with a voltage divider between V_{DDH} and V_{GND}, buffered with voltage followers.

The lower drive level, V5, is not necessarily at V_{GND}, and separate pins are used for the voltage levels when op-amps are used. A maximum voltage differential between V5 and V_{GND} of 2.5V is recommended since the driver efficiency decreases as the differential increases. Connect V5 to GND when not using op-amps.

The resistances of the voltage divider resistors should be as low as possible and within power supply constraints.

Note that fluctuations in I_{DDH} can cause dips in the V_{DDH} supply. The device will be damaged if the voltage dips below the point where the relationship V_{DDH} (V0) ≥ V2 ≥ V3 ≥ V5 ≥ V_{GND} breaks down. A stabilized power supply may be required when using the resistor network.

● Data Latch

The data latch latches the data into the level shifter on the falling edge of LP.

● Level Shifter

The level shifter converts the logic-level signals from the latch into the LCD driver input voltage levels.

● LCD Drivers

The LCD drivers generate the AC LCD drive waveforms. The output voltages are determined by the polarity of the FR signal, as shown in the following table.

Driver Output Voltage

NH	Input Data	FR	Output Voltage
H	H	H	V0 (V_{DDH})
		L	V5
	L	H	V2
		L	V3
L	X	X	V5

x = don't care

● Power-Up and Power-Down Precautions

As the driver circuitry operates at high voltage, care should be taken when applying and removing power to the SED1742 to prevent damage. If the driver supply is applied when the logic supply is either not connected or below 2.9V, excess current will flow into the SED1742 and damage the device. Normal operation is guaranteed if the correct power-up and power-down sequences are followed.

Power-Up Sequence:

Power should be applied to V_{CC} before, or at the same time as, power is applied to the driver circuitry.

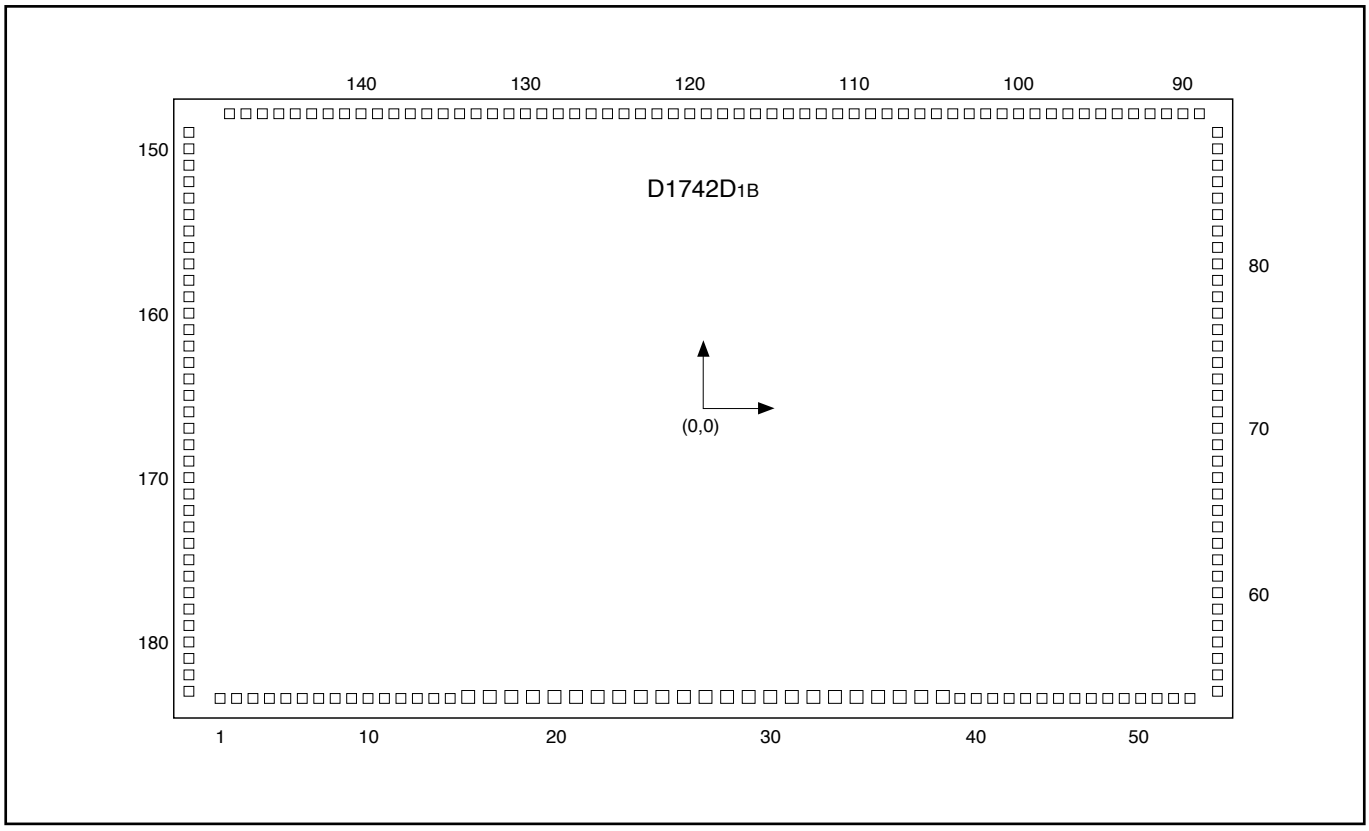
Power-Down Sequence:

Power should be removed from V_{CC} after, or at the same time as, power is removed from the driver circuitry.

The SED1742 can also be damaged if the LCD output drivers start operating before the driver supplies stabilize. INH should be held LOW to hold the driver outputs at V5 until the driver supplies have stabilized.

As an extra precaution, insert a fast-blow fuse in series with the driver supply.

■ PAD LAYOUT FOR SED1742D1B



Chip Size	7.30mm × 4.48mm
Chip Thickness	525μm ± 25μm
Pad Pitch	108μm (Min.)

Gold bump dimensions (SED1742D1B):

Size A	94 × 134 ± 20μm (pads 1~15, 39~183)
Size B	115 × 148 ± 20μm (pads 16~33, 38)
Size C	115 × 134 ± 20μm (pads 34~37)

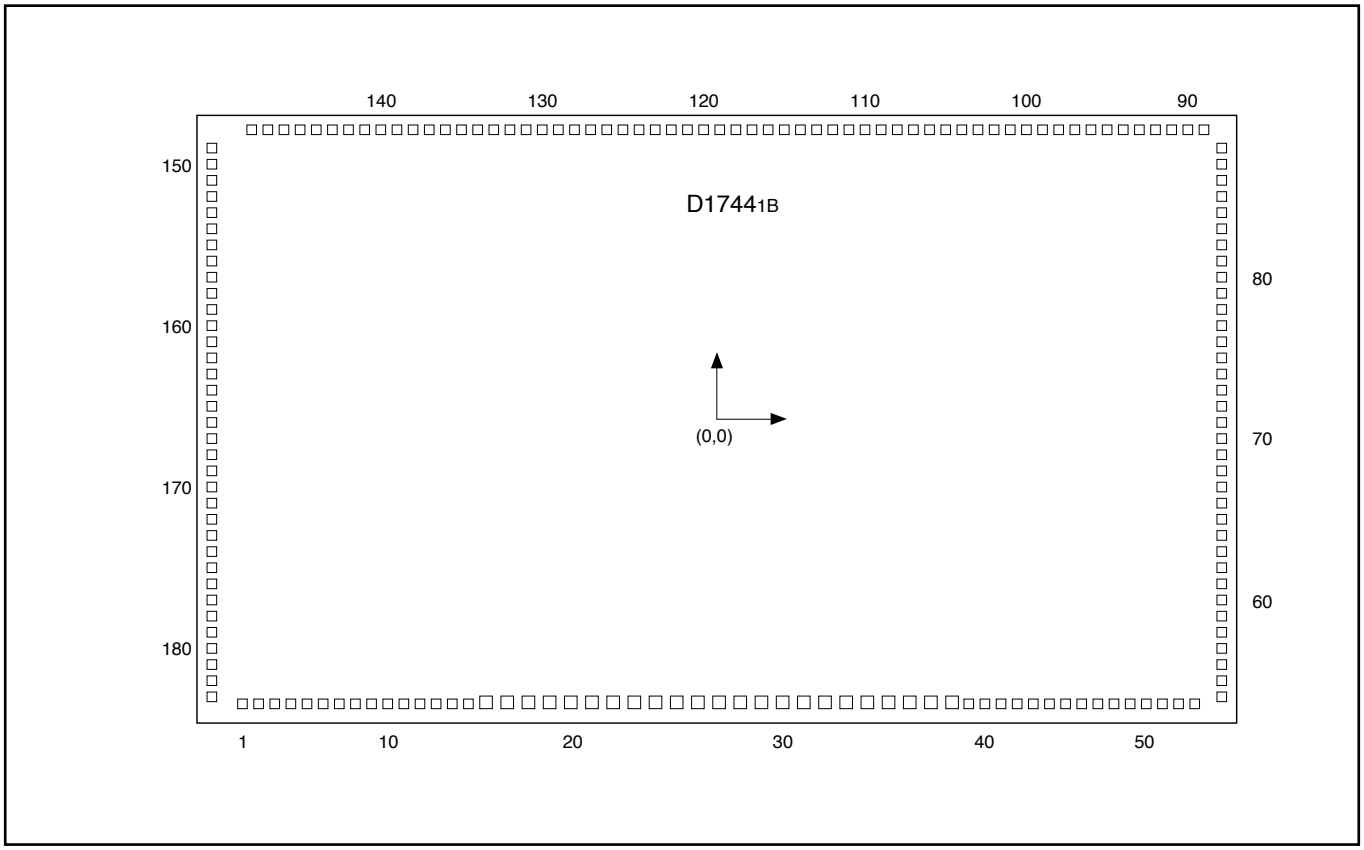
■ PAD COORDINATES

unit: μm

Pad		Coordinates		Pad		Coordinates		Pad		Coordinates		Pad		Coordinates	
No.	Name	X	Y	No.	Name	X	Y	No.	Name	X	Y	No.	Name	X	Y
1	O145	–3228	–2064	40	O1	1820	–2064	79	O40	3474	866	118	O79	54	2064
2	O146	–3120	–2064	41	O2	1929	–2064	80	O41	3474	975	119	O80	–54	2064
3	O147	–3012	–2064	42	O3	2037	–2064	81	O42	3474	1083	120	O81	–162	2064
4	O148	–2903	–2064	43	O4	2145	–2064	82	O43	3474	1191	121	O82	–271	2064
5	O149	–2795	–2064	44	O5	2253	–2064	83	O44	3474	1300	122	O83	–379	2064
6	O150	–2687	–2064	45	O6	2362	–2064	84	O45	3474	1408	123	O84	–487	2064
7	O151	–2578	–2064	46	O7	2470	–2064	85	O46	3474	1516	124	O85	–596	2064
8	O152	–2470	–2064	47	O8	2578	–2064	86	O47	3474	1625	125	O86	–704	2064
9	O153	–2362	–2064	48	O9	2687	–2064	87	O48	3474	1733	126	O87	–812	2064
10	O154	–2253	–2064	49	O10	2795	–2064	88	O49	3474	1841	127	O88	–921	2064
11	O155	–2145	–2064	50	O11	2903	–2064	89	O50	3195	2064	128	O89	–1029	2064
12	O156	–2037	–2064	51	O12	3012	–2064	90	O51	3087	2064	129	O90	–1137	2064
13	O157	–1929	–2064	52	O13	3120	–2064	91	O52	2978	2064	130	O91	–1245	2064
14	O158	–1820	–2064	53	O14	3228	–2064	92	O53	2870	2064	131	O92	–1354	2064
15	O159	–1712	–2064	54	O15	3474	–1841	93	O54	2762	2064	132	O93	–1462	2064
16	EIO2	–1550	–2058	55	O16	3474	–1733	94	O55	2553	2064	133	O94	–1570	2064
17	EIO1	–1417	–2058	56	O17	3474	–1625	95	O56	2545	2064	134	O95	–1679	2064
18	GND	–1284	–2058	57	O18	3474	–1516	96	O57	2437	2064	135	O96	–1787	2064
19	D0	–1151	–2058	58	O19	3474	–1408	97	O58	2328	2064	136	O97	–1895	2064
20	D1	–1018	–2058	59	O20	3474	–1300	98	O59	2220	2064	137	O98	–2004	2064
21	D2	–885	–2058	60	O21	3474	–1191	99	O60	2112	2064	138	O99	–2112	2064
22	D3	–752	–2058	61	O22	3474	–1083	100	O61	2004	2064	139	O100	–2220	2064
23	NC	–619	–2058	62	O23	3474	–975	101	O62	1895	2064	140	O101	–2328	2064
24	NC	–486	–2058	63	O24	3474	–866	102	O63	1787	2064	141	O102	–2437	2064
25	NC	–353	–2058	64	O25	3474	–758	103	O64	1679	2064	142	O103	–2545	2064
26	NC	–220	–2058	65	O26	3474	–650	104	O65	1570	2064	143	O104	–2653	2064
27	SHL	–87	–2058	66	O27	3474	–542	105	O66	1462	2064	144	O105	–2762	2064
28	XSCL	46	–2058	67	O28	3474	–433	106	O67	1354	2064	145	O106	–2870	2064
29	TEST	179	–2058	68	O29	3474	–325	107	O68	1245	2064	146	O107	–2978	2064
30	INH	312	–2058	69	O30	3474	–217	108	O69	1137	2064	147	O108	–3087	2064
31	LP	445	–2058	70	O31	3474	–108	109	O70	1029	2064	148	O109	–3195	2064
32	VCC	578	–2058	71	O32	3474	0	110	O71	921	2064	149	O110	–3474	1841
33	FR	711	–2058	72	O33	3474	108	111	O72	812	2064	150	O111	–3474	1733
34	V5	872	–2026	73	O34	3474	217	112	O73	704	2064	151	O112	–3474	1625
35	V3	1034	–2026	74	O35	3474	325	113	O74	596	2064	152	O113	–3474	1516
36	V2	1195	–2026	75	O36	3474	433	114	O75	487	2064	153	O114	–3474	1408
37	V0	1357	–2026	76	O37	3474	542	115	O76	379	2064	154	O115	–3474	1300
38	VDDH	1550	–2058	77	O38	3474	650	116	O77	271	2064	155	O116	–3474	1191
39	O0	1712	–2064	78	O39	3474	758	117	O78	162	2064	156	O117	–3474	1083

Pad		Coordinates		Pad		Coordinates		Pad		Coordinates		Pad		Coordinates	
No.	Name	X	Y	No.	Name	X	Y	No.	Name	X	Y	No.	Name	X	Y
157	O118	–3474	975	164	O125	–3474	217	171	O132	–3474	–542	178	O139	–3474	–1300
158	O119	–3474	866	165	O126	–3474	108	172	O133	–3474	–650	179	O140	–3474	–1408
159	O120	–3474	758	166	O127	–3474	0	173	O134	–3474	–758	180	O141	–3474	–1516
160	O121	–3474	650	167	O128	–3474	–108	174	O135	–3474	–866	181	O142	–3474	–1625
161	O122	–3474	542	168	O129	–3474	–217	175	O136	–3474	–975	182	O143	–3474	–1733
162	O123	–3474	433	169	O130	–3474	–325	176	O137	–3474	–1083	183	O144	–3474	–1841
163	O124	–3474	325	170	O131	–3474	–433	177	O138	–3474	–1191				

■ PAD LAYOUT FOR SED1744D1B



Chip Size	7.30mm × 4.48mm
Chip Thickness	525μm ± 25μm
Pad Pitch	108μm (Min.)

Gold bump dimensions (SED1744sD1B):

Size A	94 × 134 ± 20μm (pads 1~15, 39~183)
Size B	115 × 148 ± 20μm (pads 16~33, 38)
Size C	115 × 134 ± 20μm (pads 34~37)

■ PAD COORDINATES

unit: μm

Pad		Coordinates		Pad		Coordinates		Pad		Coordinates		Pad		Coordinates	
No.	Name	X	Y	No.	Name	X	Y	No.	Name	X	Y	No.	Name	X	Y
1	O145	–3228	–2064	40	O1	1820	–2064	79	O40	3474	866	118	O79	54	2064
2	O146	–3120	–2064	41	O2	1929	–2064	80	O41	3474	975	119	O80	–54	2064
3	O147	–3012	–2064	42	O3	2037	–2064	81	O42	3474	1083	120	O81	–162	2064
4	O148	–2903	–2064	43	O4	2145	–2064	82	O43	3474	1191	121	O82	–271	2064
5	O149	–2795	–2064	44	O5	2253	–2064	83	O44	3474	1300	122	O83	–379	2064
6	O150	–2687	–2064	45	O6	2362	–2064	84	O45	3474	1408	123	O84	–487	2064
7	O151	–2578	–2064	46	O7	2470	–2064	85	O46	3474	1516	124	O85	–596	2064
8	O152	–2470	–2064	47	O8	2578	–2064	86	O47	3474	1625	125	O86	–704	2064
9	O153	–2362	–2064	48	O9	2687	–2064	87	O48	3474	1733	126	O87	–812	2064
10	O154	–2253	–2064	49	O10	2795	–2064	88	O49	3474	1841	127	O88	–921	2064
11	O155	–2145	–2064	50	O11	2903	–2064	89	O50	3195	2064	128	O89	–1029	2064
12	O156	–2037	–2064	51	O12	3012	–2064	90	O51	3087	2064	129	O90	–1137	2064
13	O157	–1929	–2064	52	O13	3120	–2064	91	O52	2978	2064	130	O91	–1245	2064
14	O158	–1820	–2064	53	O14	3228	–2064	92	O53	2870	2064	131	O92	–1354	2064
15	O159	–1712	–2064	54	O15	3474	–1841	93	O54	2762	2064	132	O93	–1462	2064
16	EIO2	–1550	–2058	55	O16	3474	–1733	94	O55	2553	2064	133	O94	–1570	2064
17	EIO1	–1417	–2058	56	O17	3474	–1625	95	O56	2545	2064	134	O95	–1679	2064
18	GND	–1284	–2058	57	O18	3474	–1516	96	O57	2437	2064	135	O96	–1787	2064
19	D0	–1151	–2058	58	O19	3474	–1408	97	O58	2328	2064	136	O97	–1895	2064
20	D1	–1018	–2058	59	O20	3474	–1300	98	O59	2220	2064	137	O98	–2004	2064
21	D2	–885	–2058	60	O21	3474	–1191	99	O60	2112	2064	138	O99	–2112	2064
22	D3	–752	–2058	61	O22	3474	–1083	100	O61	2004	2064	139	O100	–2220	2064
23	NC	–619	–2058	62	O23	3474	–975	101	O62	1895	2064	140	O101	–2328	2064
24	NC	–486	–2058	63	O24	3474	–866	102	O63	1787	2064	141	O102	–2437	2064
25	NC	–353	–2058	64	O25	3474	–758	103	O64	1679	2064	142	O103	–2545	2064
26	NC	–220	–2058	65	O26	3474	–650	104	O65	1570	2064	143	O104	–2653	2064
27	SHL	–87	–2058	66	O27	3474	–542	105	O66	1462	2064	144	O105	–2762	2064
28	XSCL	46	–2058	67	O28	3474	–433	106	O67	1354	2064	145	O106	–2870	2064
29	TEST	179	–2058	68	O29	3474	–325	107	O68	1245	2064	146	O107	–2978	2064
30	INH	312	–2058	69	O30	3474	–217	108	O69	1137	2064	147	O108	–3087	2064
31	LP	445	–2058	70	O31	3474	–108	109	O70	1029	2064	148	O109	–3195	2064
32	VCC	578	–2058	71	O32	3474	0	110	O71	921	2064	149	O110	–3474	1841
33	FR	711	–2058	72	O33	3474	108	111	O72	812	2064	150	O111	–3474	1733
34	V5	872	–2026	73	O34	3474	217	112	O73	704	2064	151	O112	–3474	1625
35	V3	1034	–2026	74	O35	3474	325	113	O74	596	2064	152	O113	–3474	1516
36	V2	1195	–2026	75	O36	3474	433	114	O75	487	2064	153	O114	–3474	1408
37	V0	1357	–2026	76	O37	3474	542	115	O76	379	2064	154	O115	–3474	1300
38	VDDH	1550	–2058	77	O38	3474	650	116	O77	271	2064	155	O116	–3474	1191
39	O0	1712	–2064	78	O39	3474	758	117	O78	162	2064	156	O117	–3474	1083

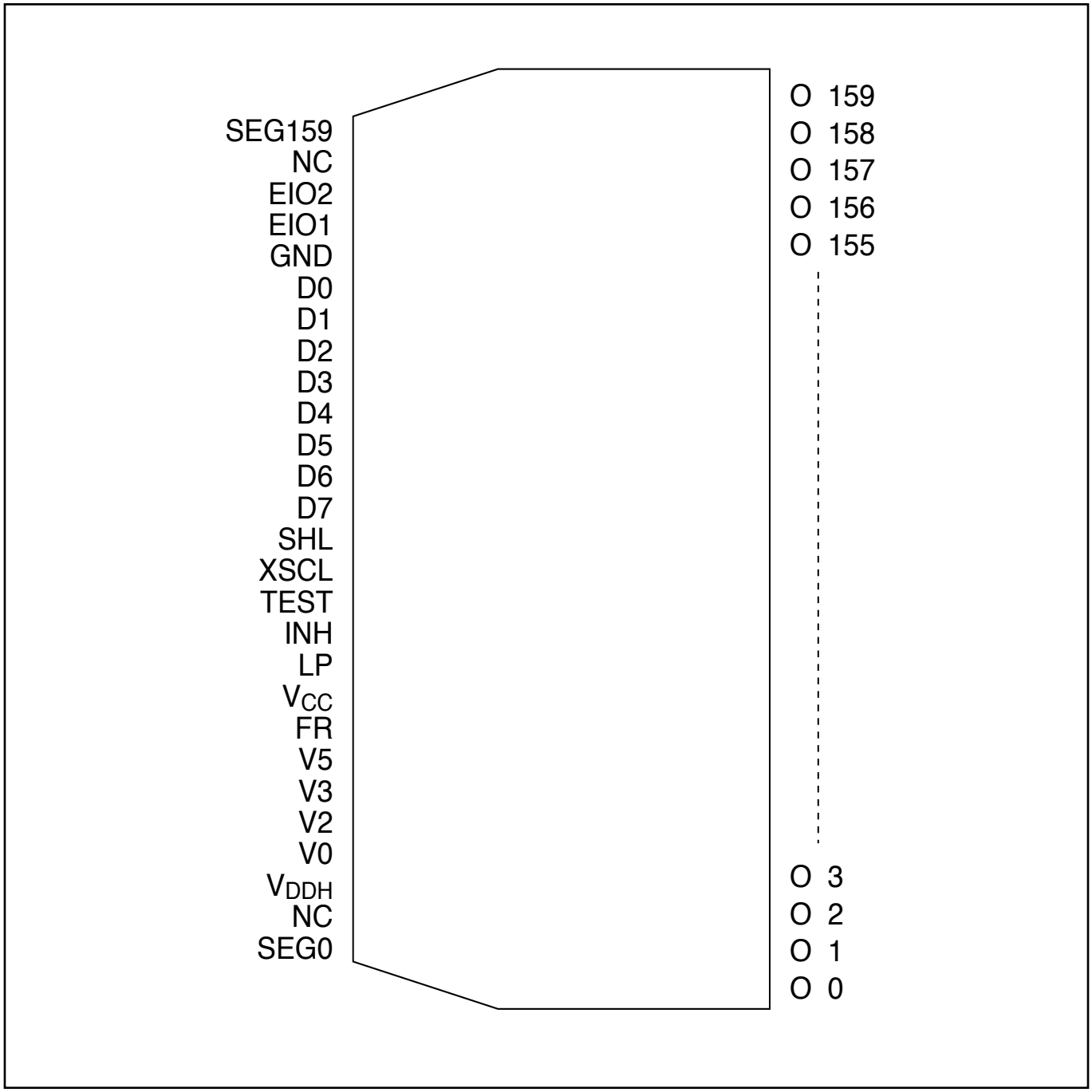
■ PAD COORDINATES (CONT.)

unit: μm

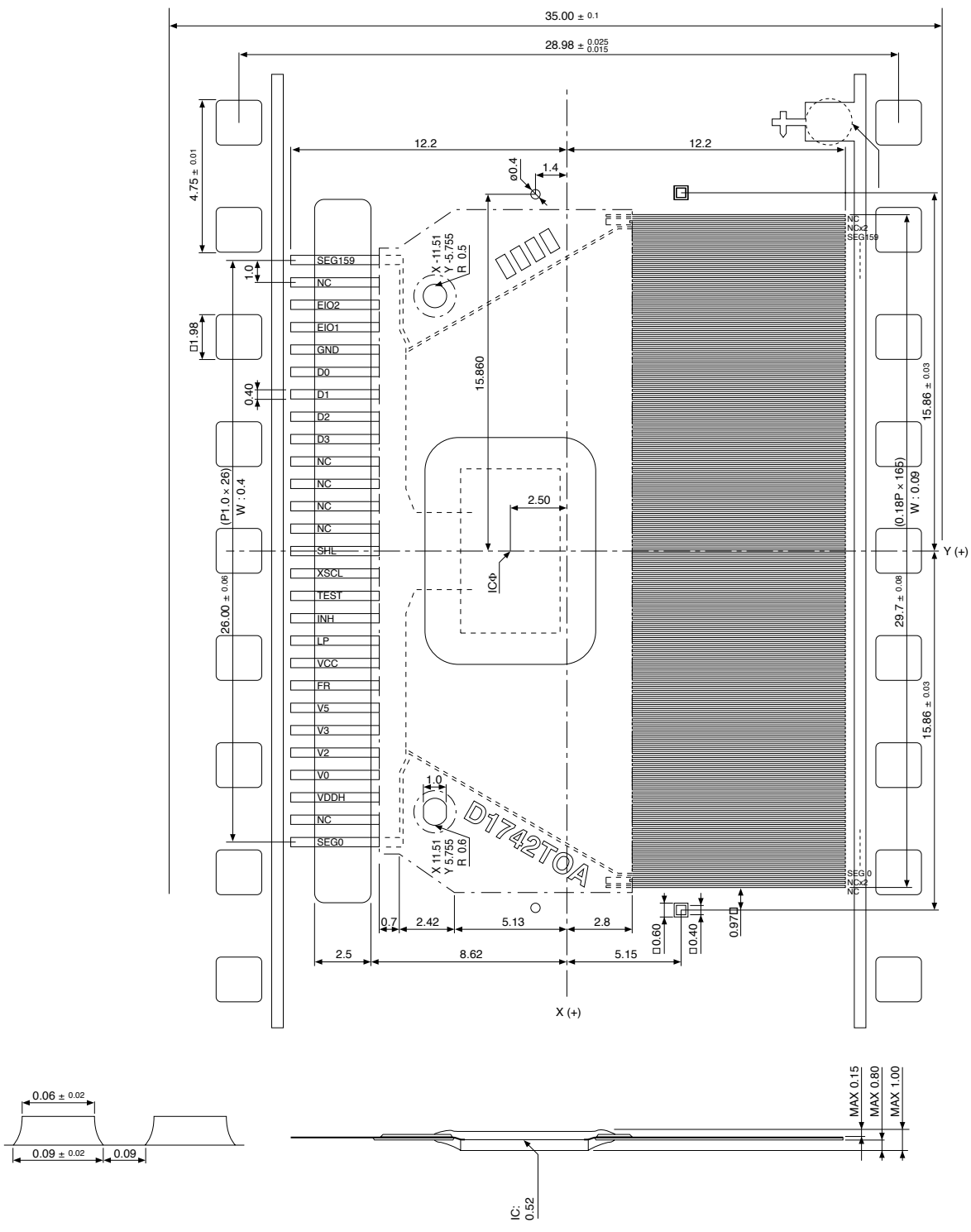
Pad		Coordinates		Pad		Coordinates		Pad		Coordinates		Pad		Coordinates	
No.	Name	X	Y	No.	Name	X	Y	No.	Name	X	Y	No.	Name	X	Y
157	O118	–3474	975	164	O125	–3474	217	171	O132	–3474	–542	178	O139	–3474	–1300
158	O119	–3474	866	165	O126	–3474	108	172	O133	–3474	–650	179	O140	–3474	–1408
159	O120	–3474	758	166	O127	–3474	0	173	O134	–3474	–758	180	O141	–3474	–1516
160	O121	–3474	650	167	O128	–3474	–108	174	O135	–3474	–866	181	O142	–3474	–1625
161	O122	–3474	542	168	O129	–3474	–217	175	O136	–3474	–975	182	O143	–3474	–1733
162	O123	–3474	433	169	O130	–3474	–325	176	O137	–3474	–1083	183	O144	–3474	–1841
163	O124	–3474	325	170	O131	–3474	–433	177	O138	–3474	–1191				

■ SED1742 TAPE-CARRIER PACKAGE

● Tape-Carrier Pinout

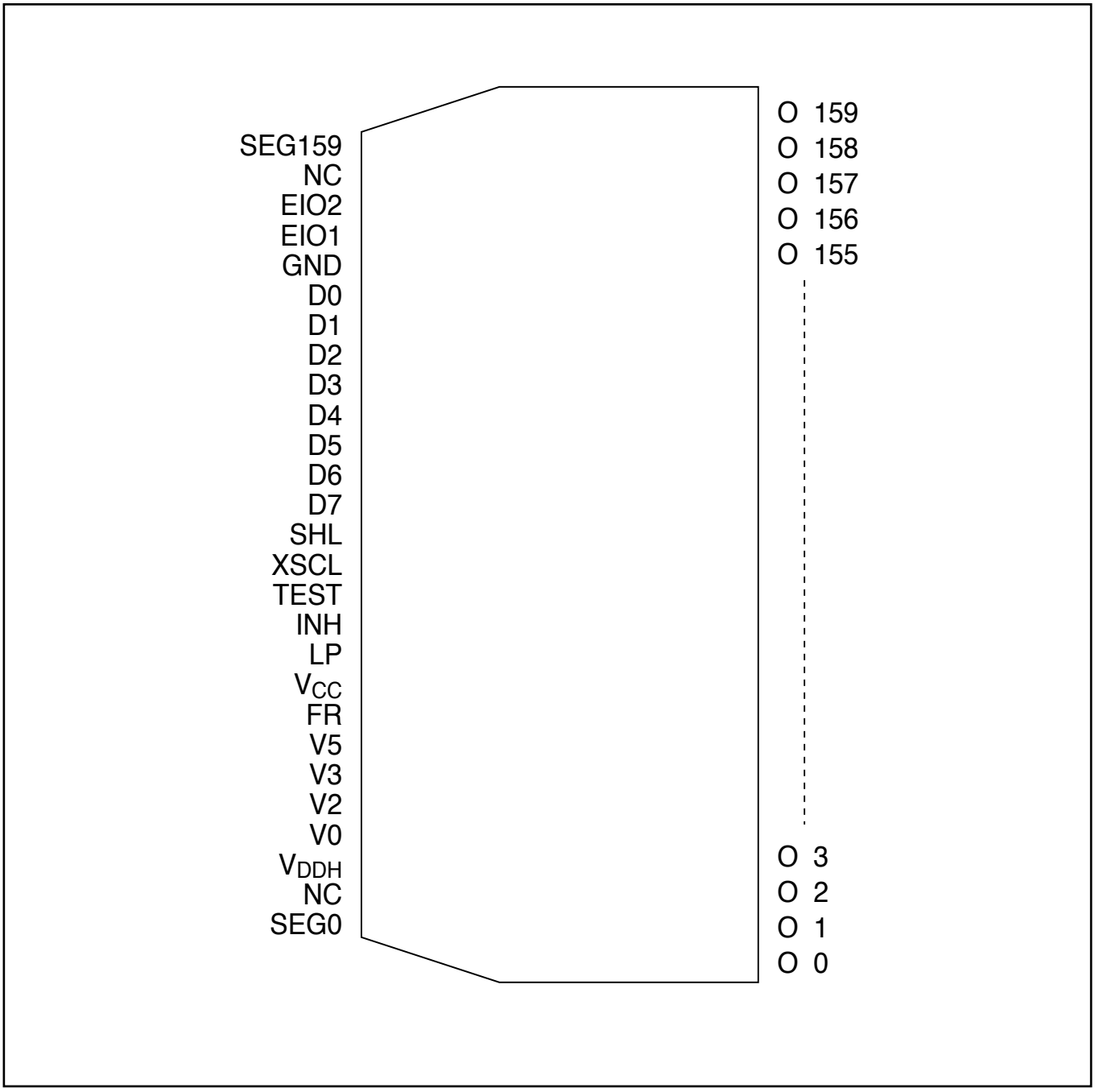


● Tape-Carrier Dimensions

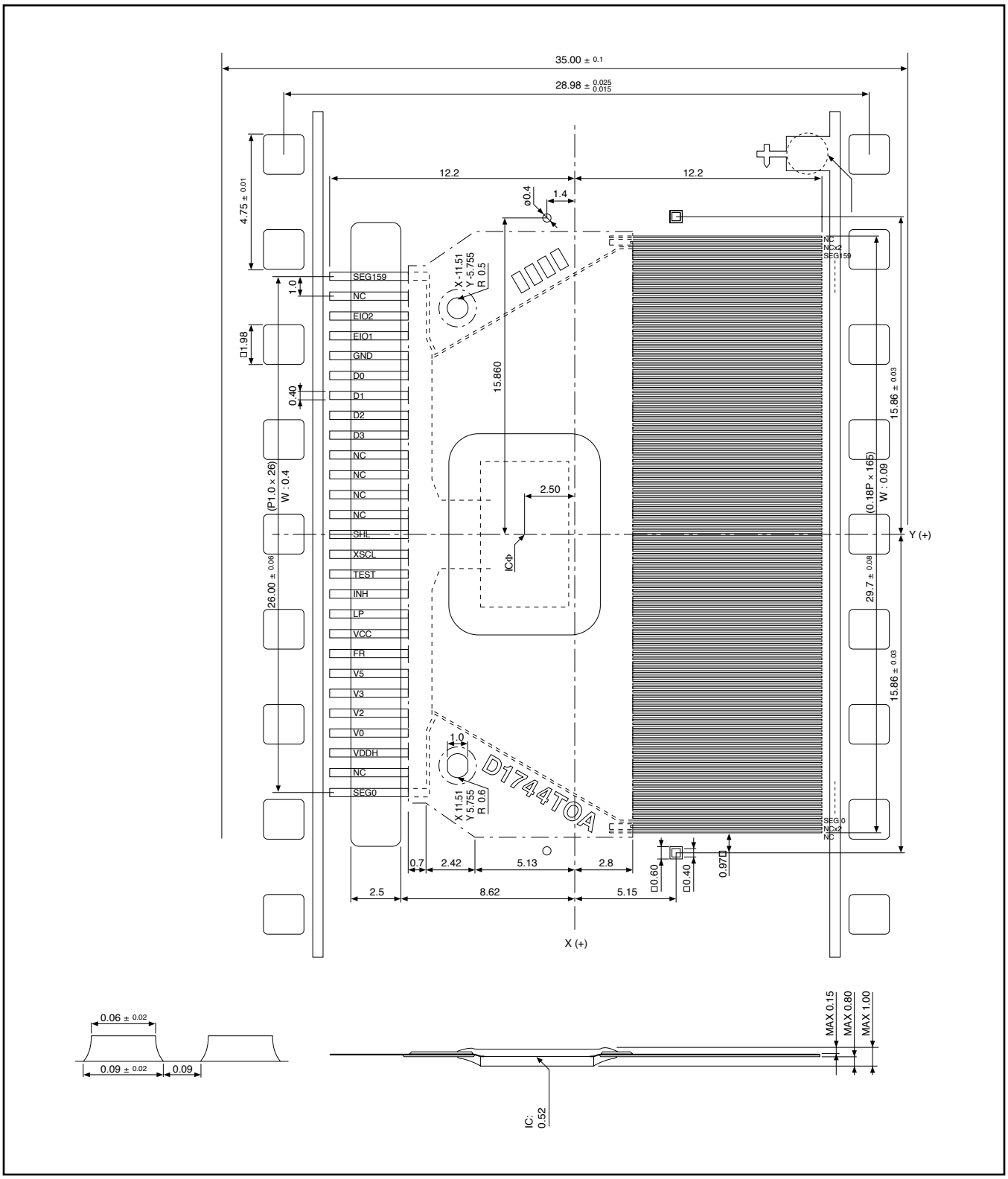


■ SED1744 TAPE-CARRIER PACKAGE

● Tape-Carrier Pinout



● Tape-Carrier Dimensions



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